REMARKS

This is a supplemental response to the Office Action mailed on November 30, 2006.

Claims 25-29, 31, 37 and 43-78 are currently pending in this application, with claims 25, 49 and 53 being independent.

No new matter has been added.

Reexamination and reconsideration in light of the following remarks are courteously requested.

Rejection under 35 U.S.C. 102 and 35 U.S.C. 103

Paragraph 6 of the Office Action includes a rejection of claims 6, 25-29, 31, 37 and 43-66 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,825,203 issued to Takeda et al. (Takeda) in view of U.S. Patent No. 5,426,447 to Lee.

Paragraph 7 of the Office Action includes a rejection of claims 6 and 25 under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 4,745,406 to Hayashi et al. (Hayashi) in view of Lee.

Paragraph 9 of the Office Action includes a rejection of claim 49 under 35 U.S.C. 102 as allegedly being anticipated by Hayashi.

These rejections are traversed at least for the following reasons.

Claims 25-29, 31, 37, 43-48 - Claims 26-29, 31, 37, 43-48 are dependent upon claim 25. Claim 25 is drawn to a liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

Takeda - All arguments presented within the Supplemental Appellant's Brief of December 13, 2005 regarding the teachings of Takeda are incorporated herein by reference. Additional arguments are provided hereinbelow.

The Office Action contends throughout that Takeda teaches the presence of driver circuits q_1-q_N.

The Office Action contends throughout that Takeda teaches the presence of driver circuit output terminals Q1, Q2.

However, Takeda *fails* to disclose, teach, or suggest that each of the driver circuits q_1-q_N has a horizontal shift register circuit and driver circuit output terminals Q1, Q2.

Instead, Takeda arguably teaches that the basic configuration of the column electrode drive circuit is the same as for the previous embodiments of this invention, *with a shift register (31)* that outputs signals to each column electrode line corresponding to the display pattern, analog switches (132), (34), condensors (33), (35) and *an output buffer amp (36)* (Takeda at column 4, lines 29-33).

Thus, Takeda *fails* to disclose, teach, or suggest each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines.

Moreover, Takeda *fails* to disclose, teach, or suggest said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines.

Lee - Lee arguably teaches that, in the external control circuits 12 that are separate from the display 14, sample capacitors 50 receive data from input circuit 64 through *shift register 49* (Lee at Figure 1, column 4, lines 47-49).

However, Lee *fails* to disclose, teach, or suggest a plurality of driver circuits, the plurality of driver circuits including at least one general driver circuit and one remainder driver

circuit, wherein each general driver circuit has a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, and the remainder driver circuit has a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals.

Thus, Lee *fails* to disclose, teach, or suggest each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines.

Moreover, Lee *fails* to disclose, teach, or suggest said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines.

Hayashi - Hayashi arguably teaches the presence of a shift register 2.

However, Hayashi *fails* to disclose, teach, or suggest a plurality of driver circuits, the plurality of driver circuits including at least one general driver circuit and one remainder driver circuit, wherein each general driver circuit has a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, and the remainder driver circuit has a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals.

Thus, Hayashi *fails* to disclose, teach, or suggest each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines.

Moreover, Hayashi *fails* to disclose, teach, or suggest said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines.

Claims 49-52, 54-66 - Claims 50-66 are dependent upon claim 49. Claim 49 is drawn to a liquid crystal display comprising:

> a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,
>
> a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and
>
> a plurality of driver circuits, each of said plurality of driver circuits having a plurality of driver circuit output terminals,
>
> a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,
>
> the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and
>
> the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Takeda - All arguments presented within the Supplemental Appellant's Brief of December 13, 2005 regarding the teachings of Takeda are incorporated herein by reference. Additional arguments are provided hereinbelow.

The Office Action contends that Takeda teaches the presence of signal lines 11-b (Office Action at page 8). The Office Action further contends that Takeda teaches the presence of signal lines Q_1, Q_N (Office Action at page 9). Clarification of what within Takeda is intended to be the signal line is respectfully requested.

The Office Action contends that Takeda teaches the presence of a plurality of driver circuits q_1-q_N (Office Action at page 9).

The Office Action contends that Takeda teaches the presence of driver circuit output terminals 37 (Office Action at page 9).

Upon review, Takeda *fails* to disclose, teach, or suggest the quantity of the alleged driver circuits q_1-q_N being defined as N/n, wherein "N" is the quantity of the alleged signal lines 11-b, Q_1, Q_N and "n" is the quantity of the alleged driver circuit output terminals 37.

Lee - Lee *fails* to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Hayashi - Hayashi *fails* to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Claim 53 - Claim 53 is drawn to a display according to claim 49, wherein said quantity of said driver circuit output terminals is set to a power of 2.

Takeda - All arguments presented within the Supplemental Appellant's Brief of December 13, 2005 regarding the teachings of Takeda are incorporated herein by reference. Additional arguments are provided hereinbelow.

The Office Action identifies item 37 of Takeda as a plurality of driver circuit output terminals (Office Action at page 9). In this regard, Takeda arguably teaches the presence of a gate circuit 37 (Takeda at Figure 1(A)).

However, Takeda *fails* to disclose, teach, or suggest the quantity of gate circuits 37 being set to a power of 2.

Lee - Lee *fails* to disclose, teach, or suggest a quantity of driver circuit output terminals being set to a power of 2.

Hayashi - Hayashi *fails* to disclose, teach, or suggest a quantity of driver circuit output terminals being set to a power of 2.

Withdrawal of these rejections and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

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Respectfully submitted,

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